

-30V P-Channel Power MOSFET

• **General Description**

It combines trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

• **Features**

- Low $R_{DS(ON)}$ to minimize conductive loss
- High GOX reliability
- Low Thermal resistance

• **Application**

- BLDC Motor driver
- DC-DC
- Load switch

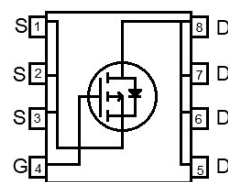
• **Ordering Information:**

Part NO.	ZM240P03M
Marking	240P03
Packing Information	REEL TAPE
Basic ordering unit (pcs)	5000

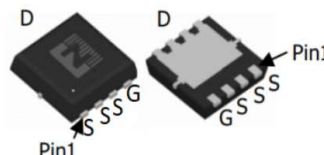
• **Absolute Maximum Ratings** ($T_C=25^\circ\text{C}$)

Parameter	Symbol	Conditions	Value	Unit
Drain-Source Voltage	V_{DS}		-30	V
Gate-Source Voltage	V_{GS}		± 20	V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	-15	A
	I_D	$T_C=75^\circ\text{C}$	-13	A
	I_D	$T_C=100^\circ\text{C}$	-10	A
Pulsed Drain Current	I_{DM}	Pulsed; $t_p \leq 10 \mu\text{s}$; $T_{mb} = 25^\circ\text{C}$;	-60	A
Total Power Dissipation	P_D	$T_C=25^\circ\text{C}$	18	W
Total Power Dissipation	P_D	$T_A=25^\circ\text{C}$	0.9	W
Operating Junction Temperature	T_J		-55 to +150	$^\circ\text{C}$
Storage Temperature	T_{STG}		-55 to +150	$^\circ\text{C}$
Single Pulse Avalanche Energy	E_{AS}	$L=0.1\text{mH}$, $V_{GS}=-10\text{V}$, $R_g=25\Omega$,	45	mJ
		$L=0.5\text{mH}$, $V_{GS}=-10\text{V}$, $R_g=25\Omega$,	95	mJ
ESD Level (HBM)	CLASS 2			

• **Product Summary**



$V_{DS} = -30\text{V}$
 $R_{DS(ON)} = 24\text{m}\Omega$
 $I_D = -15\text{A}$



DFN3*3



•Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}		-	7.1	°C/W
Thermal resistance, junction-ambient ^①	R_{thJA}		-	140	°C/W
Soldering temperature (total time<10s)	T_{sold}		-	260	°C

•Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.2	-1.7	-2.5	V
Drain-Source Leakage Current	I_{DSS}	$V_{GS}=0V, V_{DS}=-30V$			1.0	μA
Gate- Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-12A$		24	32	m Ω
		$V_{GS}=-4.5V, I_D=-8A$		37	55	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=-5V, I_{SD}=-5A$		18		S
Diode Forward Voltage	V_{FSD}	$V_{GS}=0V, I_{SD}=-12A$			1.3	V

•Dynamic characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{iss}	$f=1MHz, V_{DS}=-25V$	-	960	-	pF
Output capacitance	C_{oss}		-	106	-	
Reverse transfer capacitance	C_{rss}		-	63	-	
Gate Resistance	R_g	$f=1MHz$	-	1.9		Ω
Total gate charge	Q_g	$V_{DD}=-15V, I_D=-12A, V_{GS}=-10V$	-	12	-	nC
	$Q_g(4.5V)$		-	6.5	-	
Gate - Source charge	Q_{gs}		-	2.4	-	
Gate - Drain charge	Q_{gd}		-	2.8	-	
Turn-ON Delay time	$t_{D(on)}$	$V_{GS}=-10V, V_{DS}=-15V, R_G=3.3\Omega, I_D=-20A$	-	10	-	ns
Turn-ON Rise time	t_r		-	15	-	ns
Turn-Off Delay time	$t_{D(off)}$		-	12	-	ns
Turn-Off Fall time	t_f		-	8	-	ns
Reverse Recovery Time	t_{RR}	$V_{DD}=-20V, dI_S/dt=100A/\mu s, I_S=-20A$	-	30	-	ns
Reverse Recovery Charge	Q_{RR}		-	12	-	nC



Fig.1 Gate-Charge Characteristics

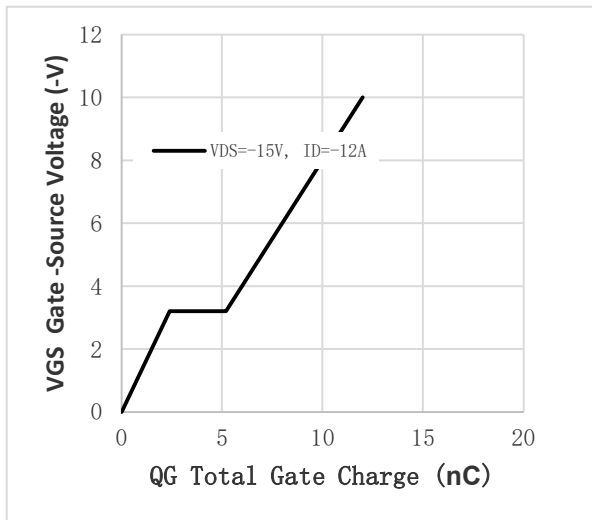


Fig.2 Capacitance Characteristics

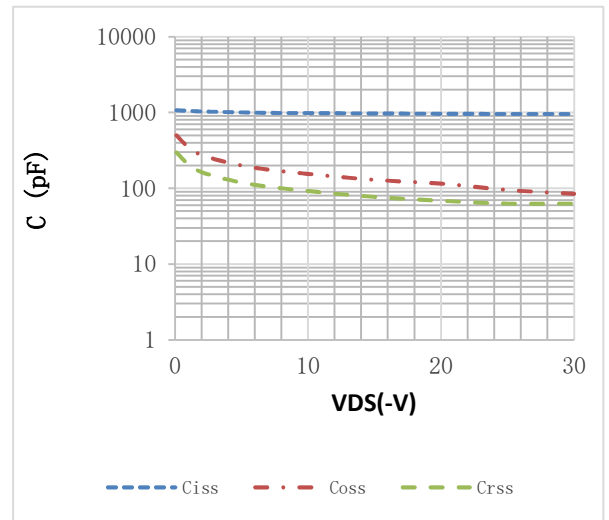


Fig.3 Power Dissipation

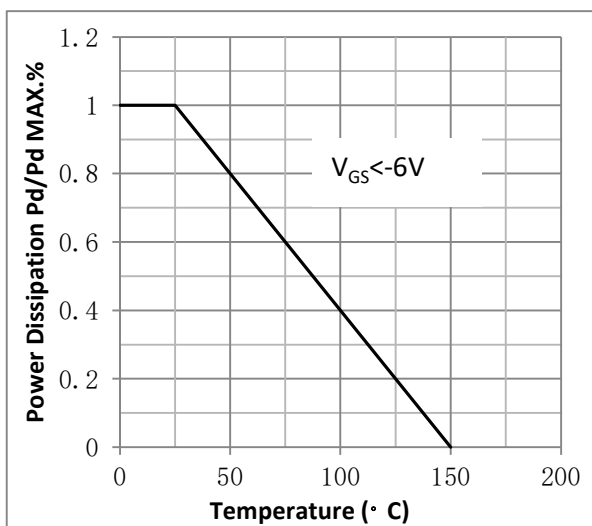


Fig.4 Typical output Characteristics

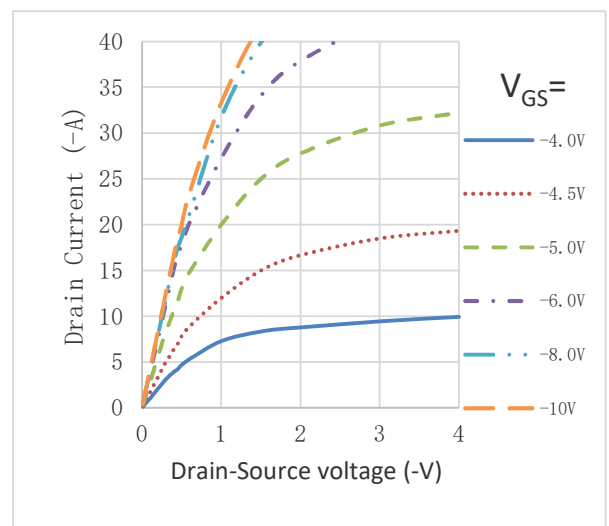


Fig.5 Threshold Voltage V.S Junction Temperature

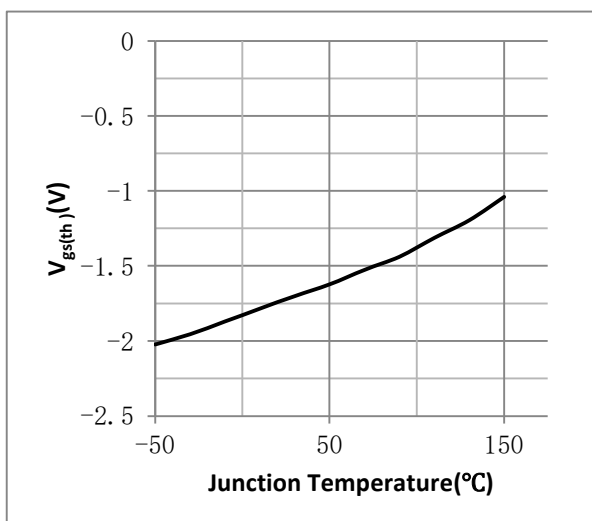


Fig.6 Resistance V.S Drain Current

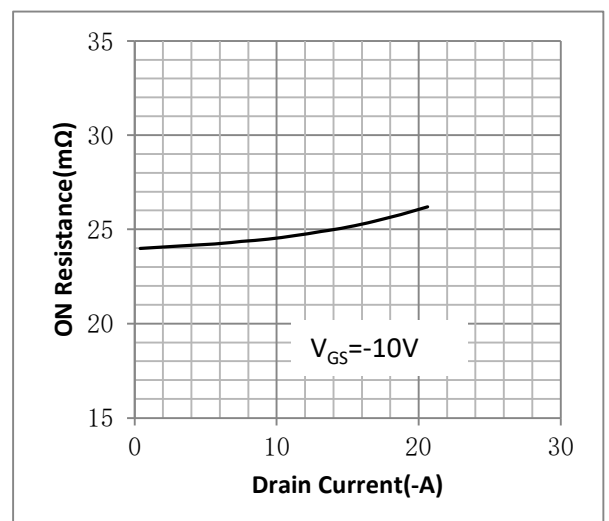


Fig.7 On-Resistance VS Gate Source Voltage

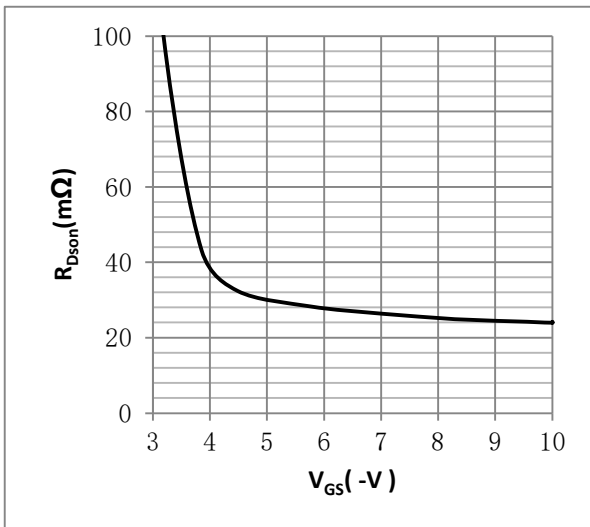


Fig.8 On-Resistance V.S Junction Temperature

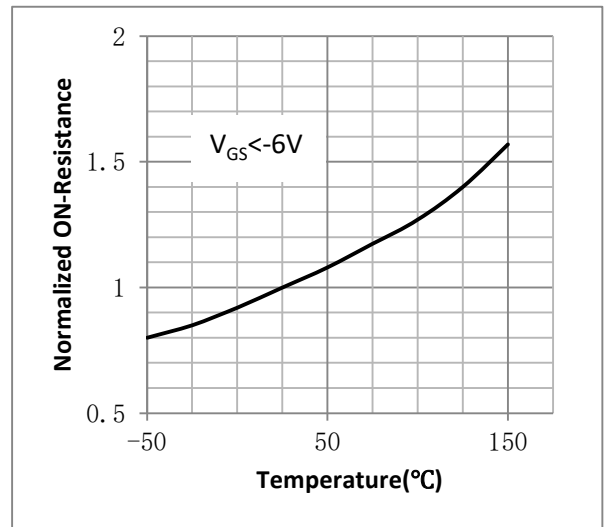


Figure 9. Diode Forward Voltage vs. Current

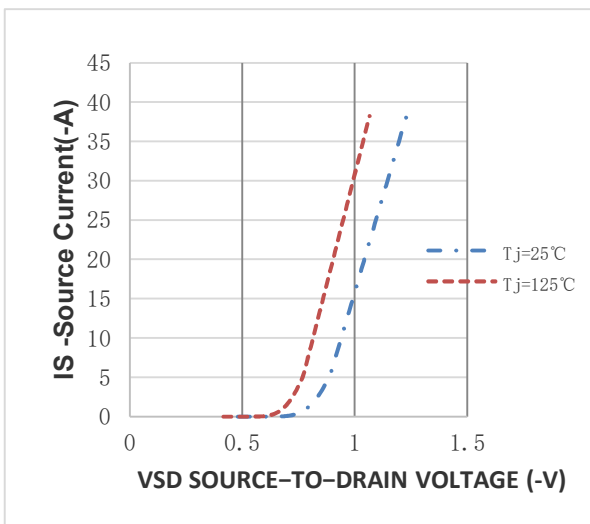


Figure 10. Transfer Characteristics

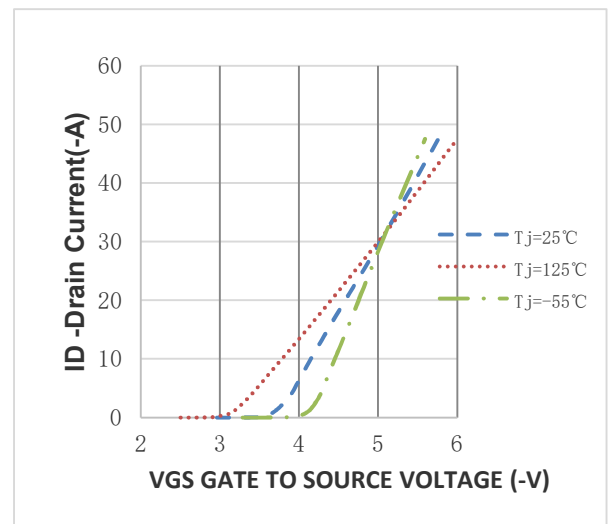


Fig.11 Safe Operating Area

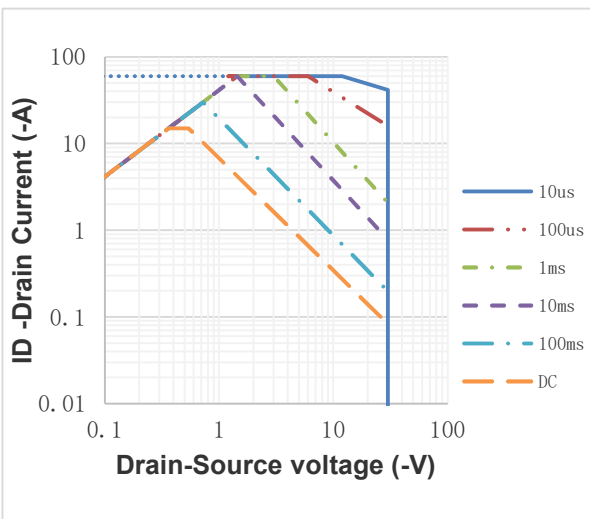
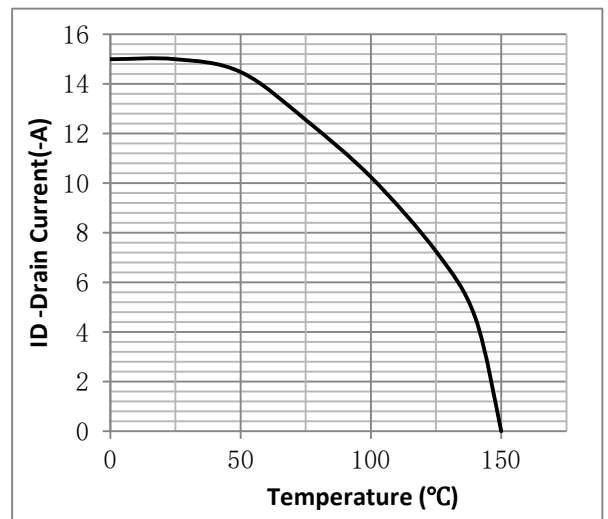
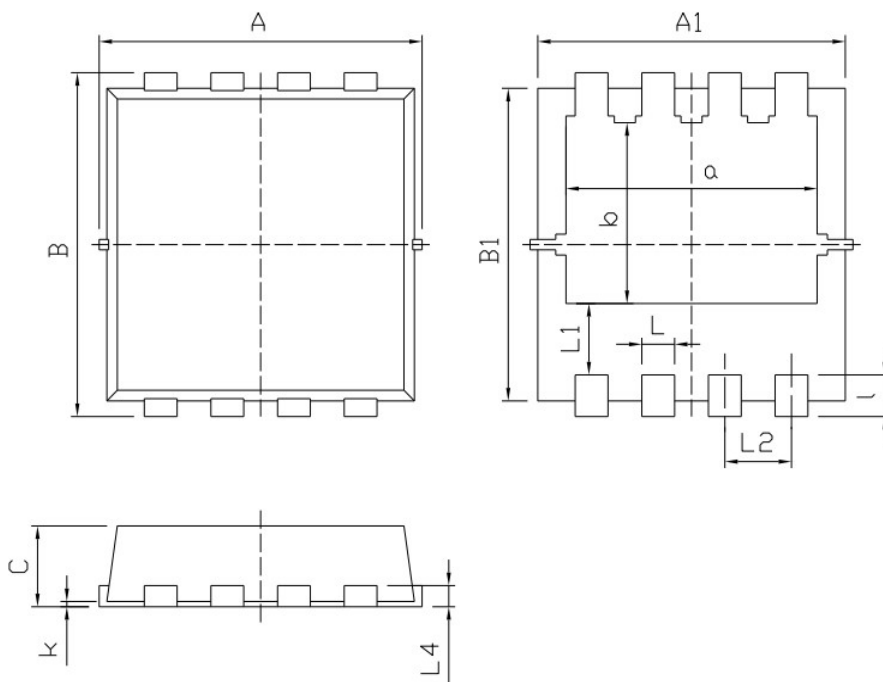


Fig.12 ID vs. Case Temperature^②



•DFN3*3 Package Outline



Dimensions In Millimeterer			
Symbol	MIN	TYP	MAX
A	3.20	3.30	3.40
A1	3.10	3.15	3.20
B	3.20	3.30	3.40
B1	2.95	3.00	3.05
C	0.75	0.80	0.85
L	0.25	0.30	0.35
L1	-	-	0.75
L2	0.55	0.65	0.75
L4	0.14	0.15	0.20
a	2.35	2.45	2.55
b	1.635	1.735	1.835
k	0.00	-	0.05
l	0.30	0.40	0.50

Note:

- ① Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;
- ② Practically the current will be limited by PCB, thermal design and operating temperature. $V_{GS} = -10V$.

Disclaimer

- Reproducing and modifying information of the document is prohibited without permission from ZMJ SEMICONDUCTORS CO.,LTD.
- ZMJ SEMICONDUCTORS CO.,LTD. reserves the rights to make changes of the content herein the document anytime without notification. Please refer to our website for the latest document.
- ZMJ SEMICONDUCTORS CO.,LTD. disclaims any and all liability arising out of the application or use of any product including damages incidentally and consequentially occurred.
- ZMJ SEMICONDUCTORS CO.,LTD. does not assume any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.
- Applications shown on the herein document are examples of standard use and operation. Customers are responsible in comprehending the suitable use in particular applications. ZMJ SEMICONDUCTORS CO.,LTD. makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.
- The products shown herein are not designed and authorized for equipments relating to human life and for any applications concerning life-saving or life-sustaining, such as medical instruments, aerospace machinery et cetera. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify ZMJ SEMICONDUCTORS CO.,LTD. for any damages resulting from such improper use or sale.
- Since ZMJ uses lot number as the tracking base, please provide the lot number for tracking when complaining.



Revision History

Version	Date	Change
A	2020.3.10	NEW
B	2022.10.30	Add ESD level
C	2023.12.28	1.Add dynamic characteristics 2.Fig1~12 modify
D	2024.5.14	Correct Cxss and Qg value
E	2025.4.29	Correct POD